

portion of the second memory cell hole, an uppermost layer of the third wire is an electrically-conductive layer and a lowermost layer of the third wire is a semiconductor layer or an insulator layer, each of the third wires including other layer of the layer structure forming the second non-ohmic element;

forming a fourth interlayer insulating layer over the third interlayer insulating layer provided with the third wires; and

forming third contacts penetrating the third interlayer insulating layer and the fourth interlayer insulating layer over the first contacts and the second contacts, and fourth contacts penetrating the fourth interlayer insulating layer over the third wires such that the third contacts and the fourth contacts are formed concurrently; and

forming upper wires on the fourth interlayer insulating layer such that each of the upper wires is connected to the third contact and the fourth contact.

11. The nonvolatile semiconductor memory device according to claim **1**, wherein each of the second wires is electrically connected to a transistor constituting a peripheral circuit of a cross-point memory formed on the substrate only via the upper wire.

12. The nonvolatile semiconductor memory device according to claim **2**, wherein each of the second wires and each of the third wires are electrically connected to a transistor constituting a peripheral circuit of a cross-point memory formed on the substrate only via the upper wire.

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